

REMARKS

Reconsideration of the present application is respectfully requested.

Claims 1-35 previously presented for examination remain in the application. No claims have been amended, no new claims have been added and no claims have been canceled.

Applicant gratefully acknowledges the allowance of claims 31-35.

Claim 11 stands rejected under 35 U.S.C. § 101 because it is considered that the claim is directed to non-statutory subject matter. In particular, it is considered that certain media, such as a computer data signal embodied in a carrier wave or a signal modulated by a carrier over a transmission medium and/or a radio frequency link, are intangible, and therefore non-statutory.

Applicant respectfully disagrees with this position and traverses the rejection. A carrier wave is an electromagnetic signal. Carrier wave claims do not fall in to any of the *per se* categories for non-statutory subject matter. In fact, the United States Patent and Trademark Office itself has previously provided illustrative examples of a carrier wave claim in its own Guidelines (see e.g. "Examination Guidelines for Computer-Related Inventions, page 38 (March 1996). Applicant is not aware of any recent changes to this policy or any legal precedent to indicate that carrier wave claims are non-statutory.

If the Examiner disagrees with this position, he is invited to contact Applicant's representative at the number provided below.

Claims 1-3, 9-13, 19-23, 29 and 30 stand rejected under 35 U.S.C. § 103(a) as being considered to be unpatentable over U.S. Patent No. 6,016,548 to Nakamura et al. ("Nakamura") in view of U.S. Patent No. 5,983,357 to Sun ("Sun").

Claim 1 includes the limitations

determining a processor state of a processor upon expiration of a system management interrupt (SMI) timer, the processor state being one of an operational state and a low power state;
loading the SMI timer with a timer value based on the processor state, the timer value being one of a first value and a second value; and
transitioning the processor to one of the operational state and the low power state according to the processor state.

(Claim 1)(emphasis added)

Applicant respectfully submits that Nakamura and Sun, alone or in combination, fail to teach or suggest the claimed features of applicant's invention including at least determining a processor state of a processor upon expiration of a system management interrupt timer.

As previously argued, and as admitted in the Office Action, Nakamura does not teach or suggest determining the processor state upon expiration of a system management interrupt (SMI) timer and transitioning the processor to one of the operational state and the low power state according to the processor state.

It is suggested in the Office Action that the Sun reference teaches this feature. Applicant respectfully disagrees.

Sun teaches an approach for computer power management approach that includes measuring a rate of communications with a device and regulating power based on that measurement (see e.g. Sun Abstract).

In the Office Action, it is asserted that Sun teaches "the SMI handler determining the usage state for each device and based on this determination, adapting the power management parameters for the device" and that this corresponds to the claimed feature of determining a processor state upon expiration of an SMI timer and then transitioning to an operational state or a low power state depending on the determined processor state. Applicant respectfully submits that this characterization is not proper.

As set forth in the specification of the current application, determining a processor state includes determining whether a processor is in a low power or operational state (see e.g. Specification, paragraphs [0039] – [0041]).

In contrast, as described at column 3, lines 14–67, including the passages identified in the Office Action as being representative of the indicated teaching, Sun discloses determining whether a device is being used at a higher or lower rate, i.e. Sun determines a device utilization rate. This cannot properly be considered to be equivalent to determining a processor state as set forth in the claims.

Thus, the combination of Nakamura and Sun, were such a combination to be made, would fail to teach or suggest the claimed features of applicant's invention including at least determining a processor state upon expiration of an SMI timer and transitioning to a given state based on that determination.

Independent claims 11 and 21 include a similar limitation. Claims 2–10, claims 12–20 and claims 22–30 depend from and further limit claims 1, 11 and 21,

respectively and thus, should also be found to be patentably distinguished over Nakamura and Sun, alone or in combination, for at least the same reasons.

Claims 4-8, 14-18 and 24-28 stand objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Based on the foregoing, applicant respectfully submits that the applicable objections and rejections have been overcome and claims 1-35 are in condition for allowance.

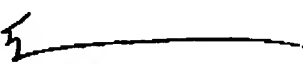
If the Examiner disagrees or believes that further discussion will expedite prosecution of this case, the Examiner is invited to telephone applicant's representative Cynthia Thomas Faatz at (408) 765-2057.

If there are any charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

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